Attachment A

Abstract of the Disclosure

A method for addressing dynamic random access memory, with providing a row address and a column address to addressing terminals of the memory, in intervals provided by a timing clock signal, to allow increasing address bus bandwidth without increasing the number of address terminals; the inventive method provides - dividing the row address and/or the column address into parts, and providing the respective parts to the address terminals at a rising, and a falling edge of the timing clock signal.